8-bit SAR ADC Design

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# **Introduction**

An 8 bit SAR-ADC is designed with given CMOS\_035 design parameters.

Design Requirements :

1. Supply Voltage : 1.8 - 3.0V
2. Input Signal : 1V full scale and 10K samples per second

10k samples per second - each sample is 100us - each bit is 100/8 = 12.5us (max)

1. Input Type : Ramp (linear rise-fall) signal & Steplike signal
2. ADC Type : SAR

Overall Structure

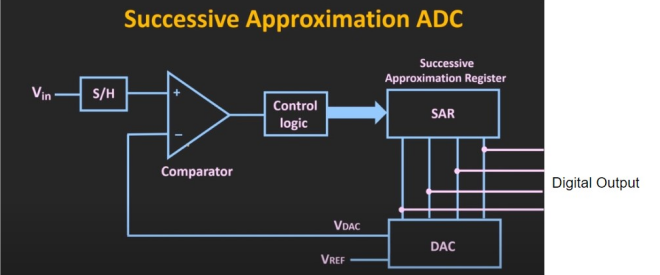


Fig. 1.1. Overall SAR-ADC Structure [[1]](#footnote-0)

SAR-ADC:

A type of analog to digital converter - convert continuous analog waveform into a discrete digital representation using binary search through all possible quantization.

Design Principle

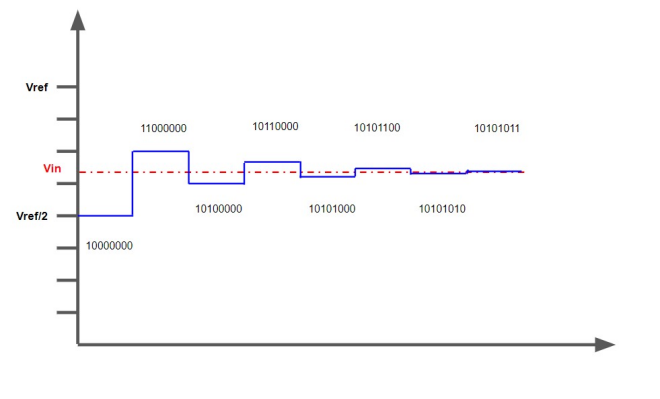


Fig1.2 Example of expected waveform

# **Design Considerations**

## Sample and Hold

The main functionality of a sample and hold circuit is to sample an analog signal and store the result in a memory element until the next instant. As stated in the design requirement, samples were taken at 10 k per second. The design consideration for the sample and hold circuit is driven by simplicity. The schematic of the sample and hold circuit can be seen in Figure 2.1. It consists of a transmission gate with the clock signal controlling the NMOS and the clock-bar signal controlling the PMOS. The design also consists of an NMOS to be used as a capacitor to store the analog voltage for a short time. The transmission gate acts as a switch to alternate the connection between the analog input and the capacitor to allow the capacitor to charge and discharge. The output of the circuit is connected to the comparator.

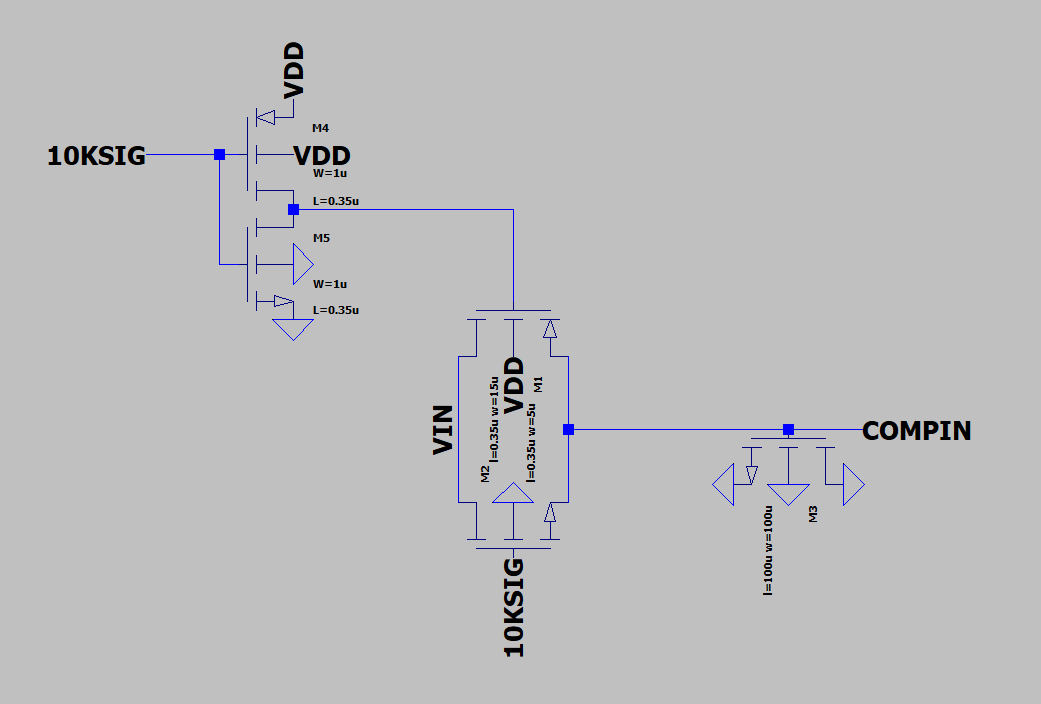


Fig. 2.1. Schematic of sample and hold circuit

In conventional designs, input and output buffers are used, but they were not used in the design as the input signal is stable and there was no observation of voltage degradation in simulations. The result from the sample and hold circuit simulation can be seen in Fig. 2.2.

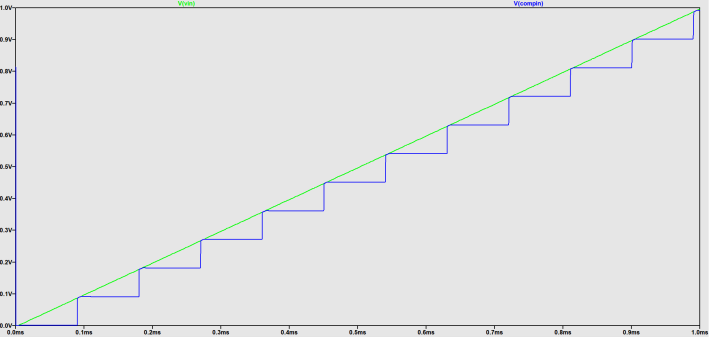


Fig. 2.2. Simulation results from the sample and hold circuit

## Comparator

The main consideration when designing the comparator is the sensitivity. The comparator has to be able to sense and compare voltage differences as low as 0.004 V.

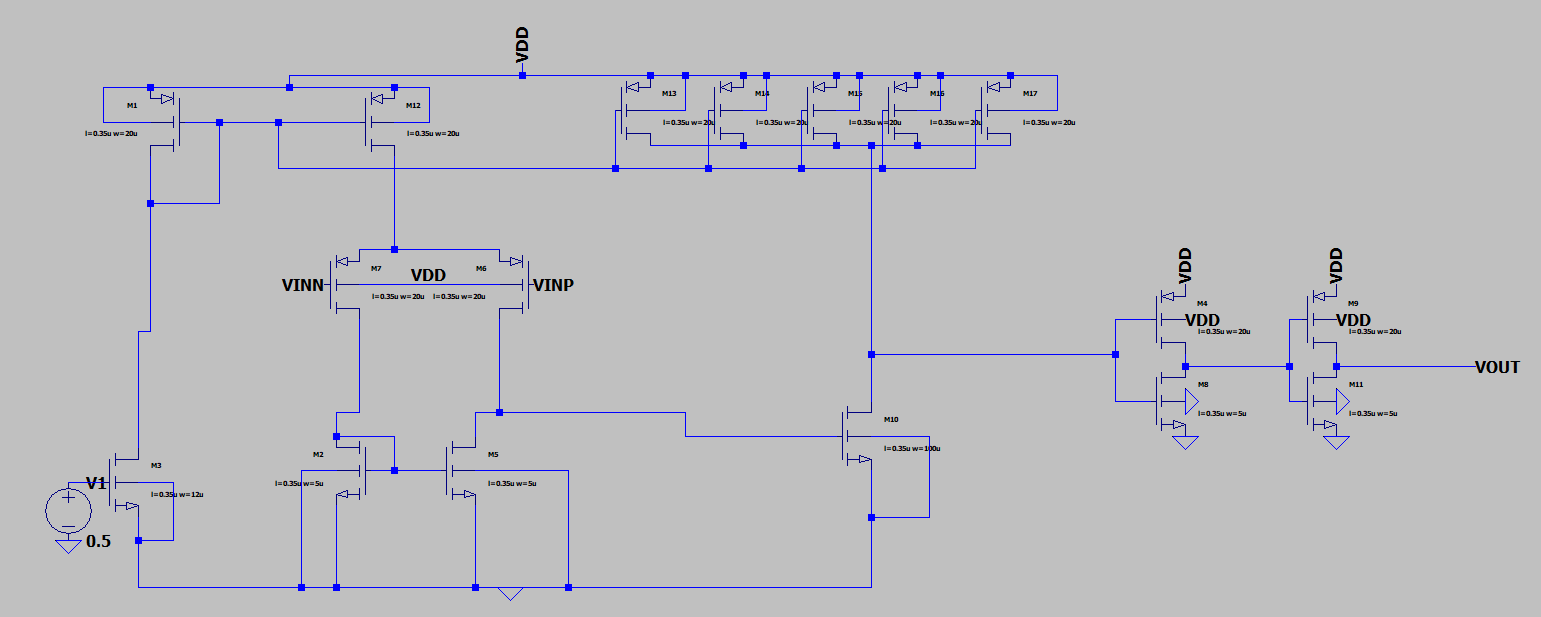


Fig. 2.3. Schematic of Comparator

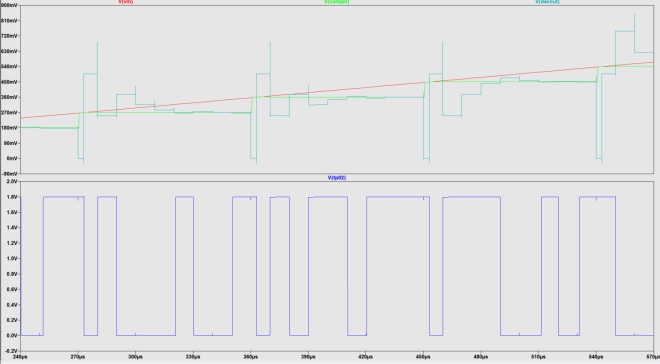
The comparator in Fig. 2.3. is made up of a differential amplifier, a push-pull output stage and a buffer.

The differential amplifier compares and amplifies the difference in voltage of the two input signals. The output from the non-inverting terminal is connected to the NMOS of the push-pull output stage, switching it off if the non-inverting input voltage is higher, and vice-versa.

The push-pull output stages, consisting of PMOS in the pull-up network and NMOS in the pull-down network, actively sink or source current to drive the output high or low depending on the output from the differential amplifier. The width of these MOSFETs was made large to increase the charging and discharging speed, thus increasing the sensitivity of the comparator.

Lastly, the buffer is implemented to maintain the output voltage level and to prevent loss of signal transfer.

From the simulated results in Fig. 2.4., the comparator was able to compare the voltage between the output of the sample and hold circuit and the output of the DAC and give the correct output accordingly.

  
Fig. 2.4. Simulated results from comparator

## Successive approximation register(SAR)

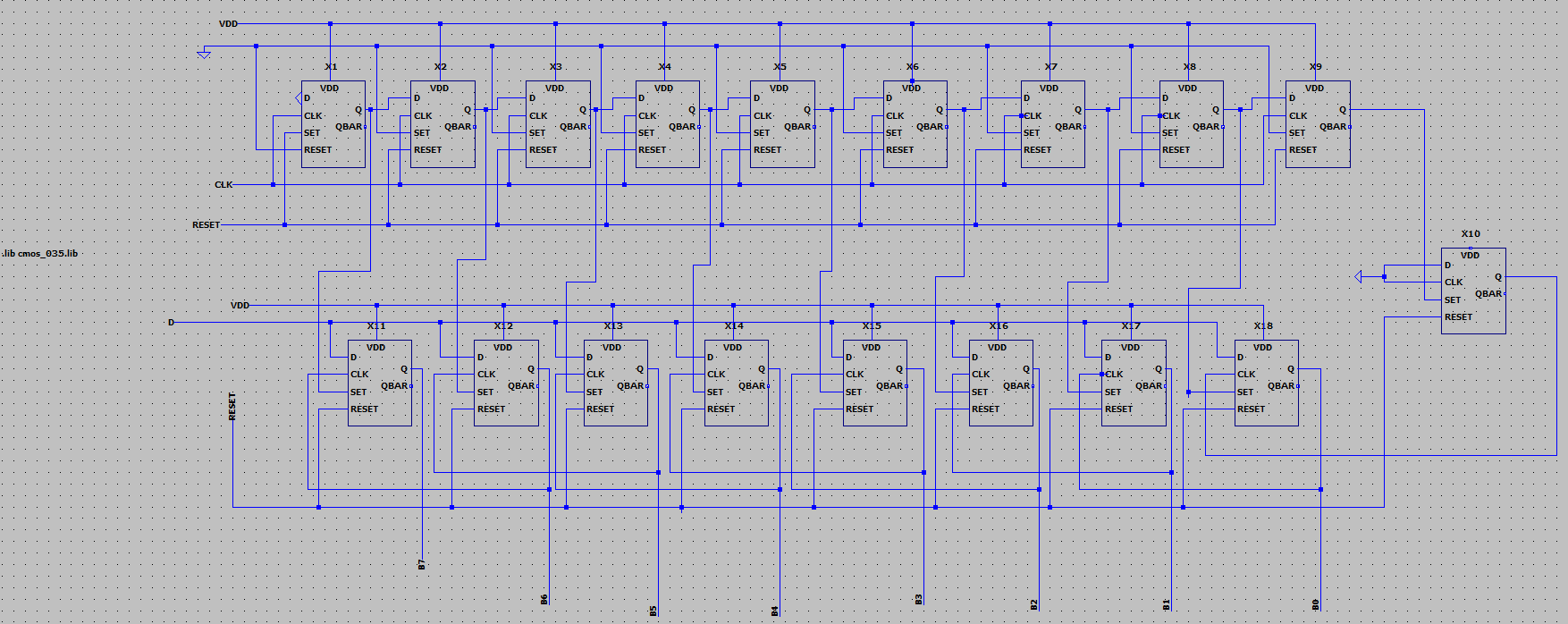
The main function of SAR is to transform the signal from comparator into digital output. Fig. 2.5. is the architecture of SAR, which consists of two rows of D latch cascades. After the reset signal is triggered, the first d latch output Q will set to high signal 1. Because of the characteristic of the register, high signal 1 will shift from left(MSB) to right(LSB). Therefore, the upper row of SAR is considered to be a shift register.

Fig. 2.5. The architecture of SAR

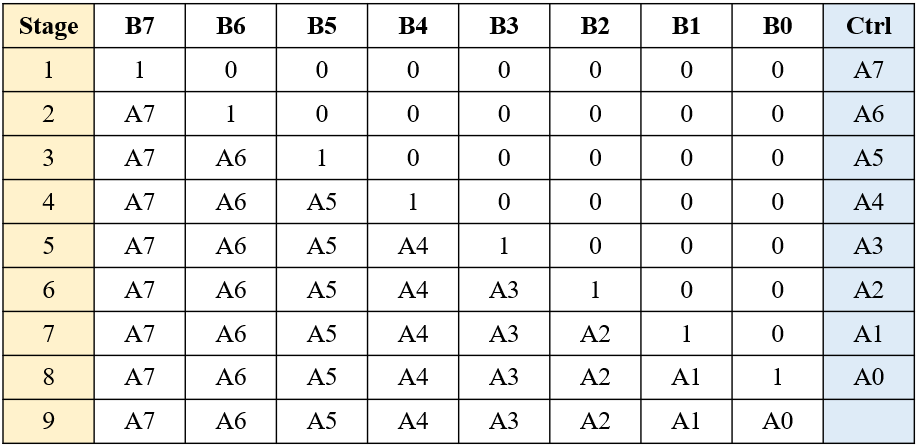
Fig. 2.6. is the operation table of the SAR. It’s obvious that after the high signal 1 is shifted to right once time, the signal from the comparator will replace the original output of the SAR.

Fig. 2.6. The operation table of SAR

In order to transform 8 bits data, it takes 9 cycles to finish the conversion. The upper part of the SAR is in Fig. 2.7. It is apparent that high signal 1 is shifted from MSB to LSB.

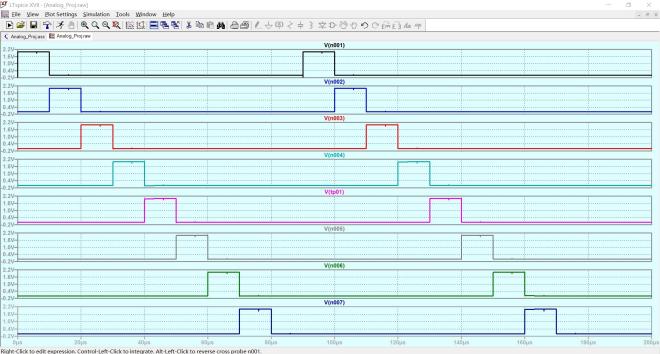


Fig. 2.8. The output of shift register

## DAC

In this project, the DAC module needs to receive the digital signal from SAR and convert the signal into analog voltage level. And then pass the analog signal to the comparator. In our case, we use R2R DAC to satisfy our design objection due to its simple design. As Fig.2.9. shows, this general DAC circuit is combined with 2 values of resistors as a ladder-like configuration of circuit. One value is R, the other is 2R, no matter how many bits are used to make up the ladder network. The real value of the resistor is decided by the design requirement. We only care about the ratio between these resistors. For n-bit R2R DAC, it will need n-1 of resistors whose value is R and n+1 of resistors whose value is 2R. Totally we need 2n of resistors for this circuit. So the

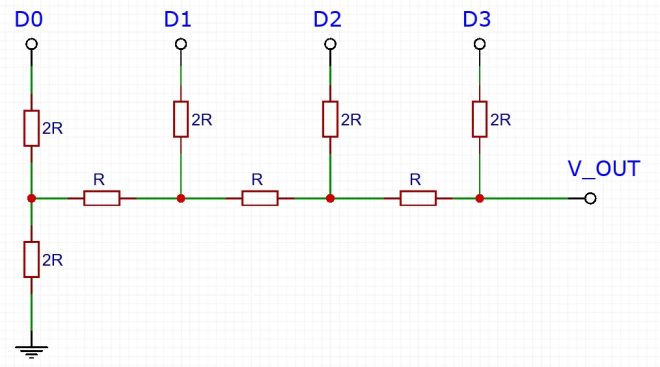
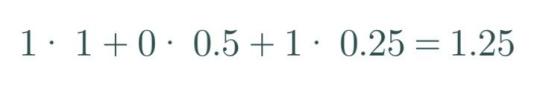
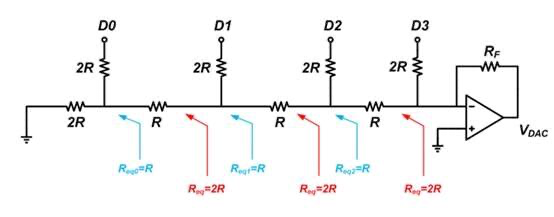


Fig 2.9. The general 4-bit R2R DAC design circuit.

After we talk about the features of R2R DAC, we are going to discuss the DAC operation principle. We take “10100000” as the digital signal input and the reference voltage as 2.0 V. We analyze the circuit by using Thevenin’s theorem to find the equivalent resistor and voltage source in each stage of DAC. First we can see the Fig.2.10.(a) to find the equivalent Thevenin resistor. We ignore the OP amplifier in this picture. In the first stage, we can consider D0 to be opened and connected to ground. As you can see that two 2R resistors parallel together, we can replace these into the equivalent R resistor. Then we can see this resistor will be connected to the next stage in series. In other words, every stage has the same equivalent resistance of the first stage. Next we consider the equivalent Thevenin voltage source. We input 2.0 V as the DAC maximum output voltage. We can see that the voltage will be divided by two 2R resistors in the first stage and the node which is between two resistances will pass half of input voltage to the next stage. So that we transform the voltage into a voltage source in Fig.2.10.(b). Each stage has the same reducing process to evaluate the voltage source and every stage voltage will be half of the last stage. It is an important theory for DAC to convert digital signal into analog signal. In the end, we can calculate the example digital input.



(a)  (b)

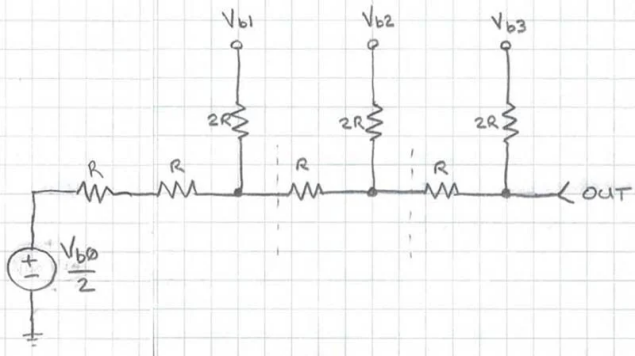


Fig 2.10. The 4-bit R2R DAC analysis using Thevenin theorem.

Now we know how R2R DAC works and designs for n-bit. We can see our 8-bit DAC full design schematic in Fig.2.11. We design 1 inverter and 1 CMOS switch for 1 bit R2R DAC input. The inverter will convert the digital input from SAR and output will control the CMOS switch. Once the converter passes “1” to switch, the PMOS will turn on and let VDD get into the R2R system. The middle circuit is the R2R system which has 16 resistors for 8 bit DAC. The resistance design parameter is below the circuit and the resistance value is 45k ohm and 90 k ohm. We need high resistance to avoid the high current which will increase the power consumption of the circuit. That’s how we realize the functionality of DAC.

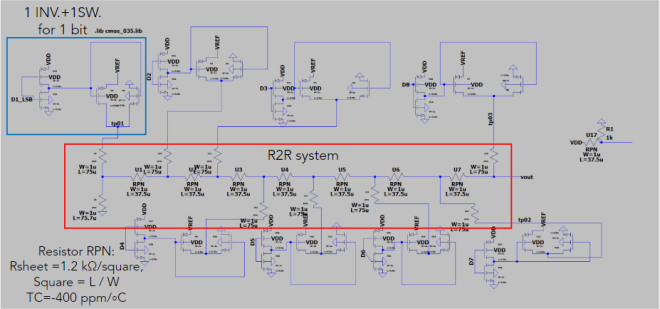
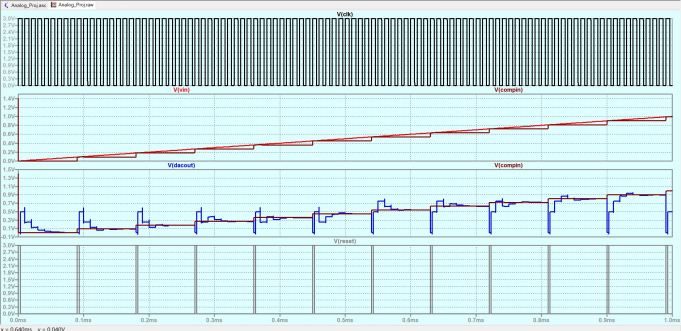


Fig 2.11. The schematic of 8 bit R2R DAC.

# **Results and Discussion**

**Output Analysis ():**



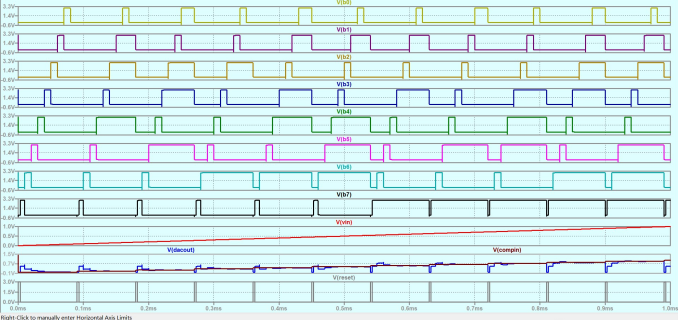
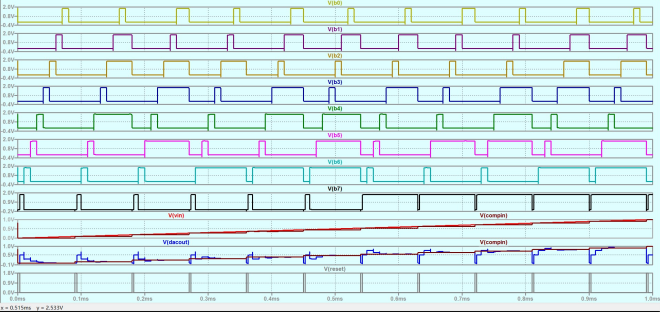


Fig3.1 Output Waveform,linear input , VDD = 3V

Fig3.2 Output Waveform,linear input , VDD = 1.8V

b7 : MSB (represents Vref \* 0.5)

b0 : LSB (represents Vref / 2^8)

Vcompin : Output from S/H circuit

Vdacout : Output from DAC circuit

**Output Analysis (step) :**

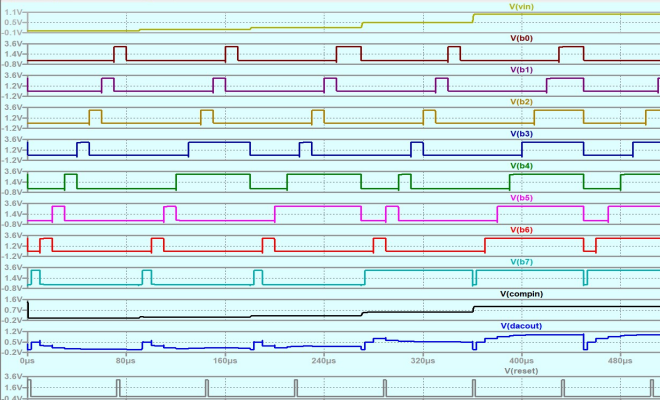


Fig3.3 Output Waveform,step input , VDD = 3V

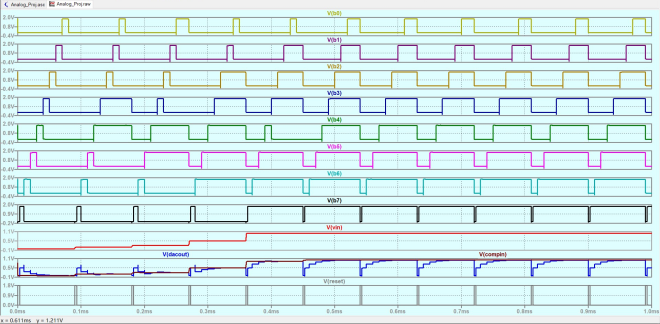
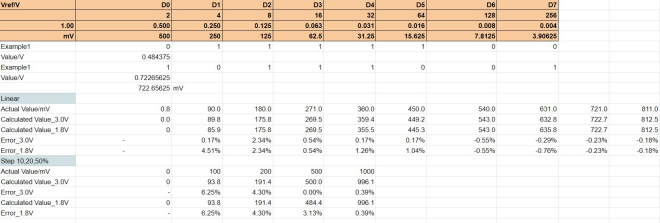
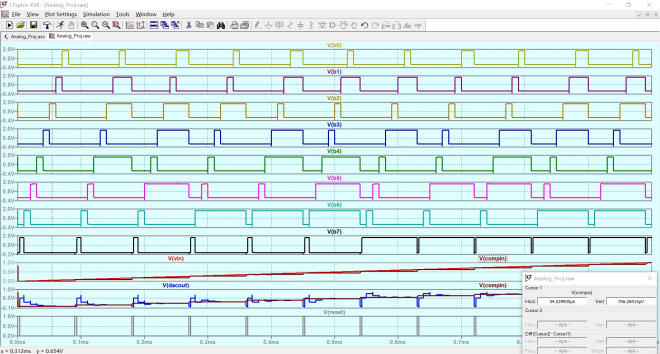


Fig3.4 Output Waveform,step input , VDD = 1.8V

**Results Analysis:**



Due to the initial setup of the signal, the output from S/H circuit is delayed and holds at 3.6mV. A delayed input signal is also tested and the output waveform is shown below. The initial sample value is kept closer to 0. And each increase is around 90mV.



**Observations:**

1. Accuracy increases with the increases of sampling voltage
2. This design can perform well with 1.8-3.0V input.

# **Conclusions**

This design performs well generally with the given ideal input sources. For application, it needs to capture the noise from the source other than quantization noise. Such calibration needs to be realized and tested. The performance also needs to be improved in terms of power consumption. There are a few transistors used in the design with Width = 100 um , which may not be applicable in real design and manufacturing.

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